Current US Cross Reference

Classification - CCXR (1):

345/426

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SHADING

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[45] Date of Patenti Jul. 5, 1994 FOREIGN PATENT DOCUMENTS 96-061874 5/1981 Japan \_ 58-117787 7/1983 Japan \_ nd: May 28, 1994

LCI HDAN 8/171; HDAN 5/275

LCI HDAN 8/171; 144/782; 144/790;

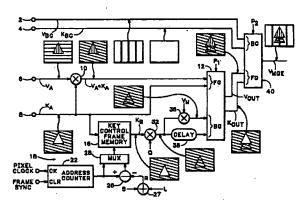
144/782; 144/791; 144/711; 145/119; 195/125

M of Search 1514/22 12 CK, 21 C, 151/12 PP, 113, 115, 160, 140/729; 195/118, 116, 118; 382/43, 34; 345/139; HDAN 5/27; 5/275 ABSTRACT [58] Field of Se

[27] A shaped video having an imput key control signal associated therewith is processed by carrying out a first operation on the input key control signal to provide a first processed signal, carrying out a second operation on the first processed signal, carrying out a second operation on the first processed signal to provide a second processed signal, and combining the shaped video signal and the second processed signal to provide as enoutput video signal. One of the first and second operations comprises translation. In this manner, a simulated shadow is added to the shaped video signal. U.S. PATENT DOCUMENTS 4,041,537 8/1977 Rayner et al. ... 4,109,278 8/1978 Mendrah et al. ... 4,589,581 8/1987 Jackson ... 4,851,912 7/1989 Jackson et al. ...

10 Claims, 4 Drawing Sheets

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Detailed Description Text - DETX

The address signals used for writing to and reading from the frame memory 16
are generated by an address
signal generator 18 comprising an address counter 22 that counts pixel clock pulses and is cleared by a frame sync pulse.
Therefore, the output of the address counter is representative of the position representative of the position (x,y) in the video raster of the pixel currently being received by the frame by the frame memory 16. The address counter 22 counts lines (vertical) and pixels (horizontal) separately, and its output is applied to the addend input of a subtraction circuit 26. An adder 27 receives a latency signal L and a shadow offset signal S and provides a resultant offset signal R, which is the sum of the latency signal L and the shadow offset signal S, to the subtrahend input of the subtraction circuit 26.

Detailed Description Text - DETX

(7):
The latency signal L represents the number of pixel clock delays between the output of the memory 16 and the background inputs of the combiner 12. The latency signal L may be considered as defining a vector F2 (2.7) = #8 (2.1)

where  $F_{S}(x,y)$  is the ratio of the average intensity when the fine intensity verteion near the pixel F(x,y) is cancaded to the transfert intensity. Therefore, when the average intensity near the part which has the similar texture as that in the object area and has no thabove and shade because it is exposed fully to light is set as a standard intensity,  $F_{S}(x,y)$ indicates the deeper of thatove and shade is the location.

estime. Next, an image wherein the color vectors of all or a part ' the pixals in this area are changed is generated or terrally inputed and obtained. The color vector of the pixal P (a, y) in the above object 60 ca of this new image is assumed as Cm (Formula 11).

where Rm (x, y), Gm (x, y), and Bm (x, y) are scalars indicating the R component, G component, and B compo-

 $Cor(x,y) = \begin{bmatrix} \frac{2}{3} cr(x,y) \\ Cor(x,y) \\ \frac{2}{3} cr(x,y) \end{bmatrix}$ 

Q C M E

onto the pixel P (x, y), it is necessary to multiply gm (x, y) by the coefficient indicating the information of shadow and shade at the location. When the intensity obtained by simulation is assumed as gr (x, y), it is represented by Formula 18. A symbol gr (x, y) is a scalar.

